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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,465	07/06/2005	Shinji E. Mino	L7990.05102	8930
52989	7590	06/14/2006	EXAMINER	
STEVENS, DAVIS, MILLER & MOSHER, LLP 1615 L. STREET N.W. SUITE 850 WASHINGTON, DC 20036			ARORA, AJAY	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/541,465

Applicant(s)

MINO ET AL.

Examiner

Ajay K. Arora

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 7/6/2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7/6/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates (US 5,338,625), hereinafter Bates, in view of Rezvani (US 6,663,037), hereinafter Rezvani.

Regarding Claim 1, Bates (refer to Figure 1 and 3) teaches a battery mounted integrated circuit device, comprising: (1) a semiconductor substrate (22); (2) a solid state battery (10) mounted on said semiconductor substrate (Col. 3, lines 23-27); (3) an integrated circuit (16) mounted on said semiconductor substrate; said solid state battery (refer to Figure 3) comprising a positive electrode, a negative electrode (cathode 24 and anode 28), and a solid electrolyte (26) disposed between said positive electrode and said negative electrode. However, Bates does not teach the claimed first and second

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diffusion layers and their configuration. Rezvani teaches a method for isolating circuits in one region of the substrate (110) from another region of the substrate (120) using substrate n-wells, wherein the isolation structure comprises: a first diffusion layer (140), containing an N-type impurity, formed between a first region (110) of semiconductor substrate and another region (120) of the semiconductor substrate; and a second diffusion layer (130), containing an N-type impurity, formed below said region (140) of said semiconductor substrate, and overlapping with said first diffusion layer. Figure 1B of Rezvani further teaches that the concentration of said N-type impurity ( $n^+$ ) in said first diffusion layer (140) is higher than the concentration of said N-type impurity ( $n$ ) in said second diffusion layer (140). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Bates with the isolation structure of Rezvani so that the battery mounted integrated circuit device includes a first diffusion layer, containing an N-type impurity, formed between a region of said semiconductor substrate where said solid state battery is mounted and an region of said semiconductor substrate where said integrated circuit is mounted; and a second diffusion layer, containing an N-type impurity, formed below said region of said semiconductor substrate where said solid state battery is mounted, and overlapping with said first diffusion layer, and further that the concentration of said N-type impurity in said first diffusion layer is higher than the concentration of said N-type impurity in said second diffusion layer. The ordinary artisan would have been motivated to modify Bates for at least the purpose of fabricating circuits of diverse functionality (such as a solid state thin film battery and an analog IC) on a single integrated circuit (see Rezvani, Col.

1, lines 10-13), while enabling isolation between the two (see Rezvani, Col. 1, lines 47-50).

Regarding Claims 2 and 3, Rezvani teaches a high concentration of said N-type impurity in said first diffusion layer (higher than second diffusion layer) but does not expressly teach that: a) the concentration is not less than  $1 \times 10^{19}$  atoms/cm<sup>3</sup> (as in Claim 2) or b). that the ratio of the concentration of said N-type impurity in said first diffusion layer to the concentration of said N-type impurity in said second diffusion layer is not more than  $1 \times 10^5$  (as in Claim 3). However, Rezvani teaches that among other things, the concentration of said N-type impurity and the relative concentration of N-impurity in first and second diffusion layers affects isolation achieved and that various doping schemes may be used (Col. 3, lines 38-58). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Bates so that: a) the concentration of said N-type impurity in said first diffusion layer is not less than  $1 \times 10^{19}$  atoms/ cm<sup>3</sup> and/or b). that the ratio of the concentration of said N-type impurity in said first diffusion layer to the concentration of said N-type impurity in said second diffusion layer is not more than  $1 \times 10^5$ . The ordinary artisan would have been motivated to modify Bates for at least the purpose of design considerations to achieve optimal isolation for the specific devices being isolated and their associated circuit parameters like operating voltage and breakdown voltage.

Regarding Claim 4, Rezvani (see Figure 4B) teaches that the said first diffusion layer and said second diffusion layer have a positive potential (Col. 6, lines 28-39).

Regarding Claim 5, Rezvani teaches that the said positive potential is not less than a potential of said positive electrode with respect to said negative electrode (Col. 4, lines 1-6).

Regarding Claim 6, Rezvani (see Figure 1A and 1B) teaches that said first diffusion layer (140) surrounds the region (110) to be isolated, which can be the region where solid state battery is mounted (as explained for Claim 1).

Regarding Claim 7, Rezvani (see Figure 1B) teaches the battery mounted integrated circuit device further comprising a wiring layer (wiring connected to 180) for connecting said first diffusion layer (140) with the outside.

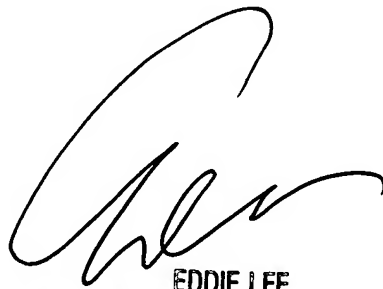
Regarding Claim 8, Rezvani (see Figure 1B) teaches a potential controlling section (180) for controlling a potential to be applied to said first diffusion layer and said second diffusion layer.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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